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10/777,576	02/12/2004	Toshiharu Furukawa	ROC920030271US1	6152

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EXAMINER	
NADAV, ORI	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,576	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-13,15-20,34-44 and 46-53* is/are pending in the application.

4a) Of the above claim(s) *9-13,20,36-42 and 49-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,15-19,34,35,43,44,46-48,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 5-8, 15-19, 34-35, 43-44, 46-48 and 52-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a gate electrode including a vertical sidewall and a gate dielectric, as recited in claims 1 and 43, are unclear as to how a gate electrode can include a gate dielectric.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5-8, 15-19, 34-35, 43-44, 46-48 and 52-53, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (6,566,704) in view of Ochipinti et al. (2004/0027889).

Regarding claims 1 and 43, Choi et al. teach in figure 3F and related text a circuit comprising:

an interconnected plurality of semiconductor device structures arranged in an array (see figure 2I), each of said semiconductor device structures further including

a gate electrode 20 including a vertical sidewall and a gate dielectric 30 disposed on the vertical sidewall,

a plurality of semiconducting carbon nanotubes (see paragraph [0027]) each #100 having a channel region disposed adjacent to said vertical sidewall of said gate electrode and each including opposite respective first and second ends,

a first contact 40 electrically coupled with said first end of each of said semiconducting carbon nanotubes,

and a second contact 50 electrically coupled with said second end of each of said semiconducting carbon nanotubes.

Choi et al. do not depict in figure 3F plurality of nanotubes and do not explicitly state in the embodiment of figure 3F that each of said semiconductor device structures is arranged as an interconnected plurality of semiconductor device structures in an array characterized by a plurality of rows and a plurality of columns.

Choi et al. teach in the embodiment of figure 4B that each of said semiconductor device structures is arranged as an interconnected plurality of semiconductor device structures in an array characterized by a plurality of rows and a plurality of columns.

Ochipinti et al. teach that a memory device conventionally uses an array characterized by a plurality of rows and a plurality of columns (paragraph [0010]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an array characterized by a plurality of rows and a plurality of columns in the device of figure 3F of Choi et al.'s device in order to use the device in a practical application which requires plurality of unit cells and in order to simplify the processing steps of making the device by using conventional rows and columns array matrix.

Regarding claims 3-8, 34, 37, 44-48, Choi et al. teach said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube, and

a plurality of semiconducting carbon nanotubes extending vertically at a plurality of locations adjacent to said vertical sidewall of said gate electrode (see figure 4B), wherein

said first contact includes a catalyst pad (the first contact is the catalyst pad) characterized by nanocrystals of a catalyst material, wherein

said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance (the electrical-conductivity enhancing substance is the material of said at least one semiconducting carbon nanotube), and

an insulating layer disposed between said first contact and said gate electrode 20 for electrically isolating said first contact from said gate electrode, and

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

Regarding the process limitations recited in claims 5-6, 34 and 46 ("nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube", and "an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 15-18, prior art teach a memory circuit comprising:

a plurality of word lines each electrically intreconnecting said gate electrode of each of said plurality of semiconductor device structurers located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of columns of said array, wherein

each of said plurality of word lines comprises said gate electrode of each of said plurality of semiconductor device structures located in said corresponding one of said plurality of rows of said array, wherein

each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of rows of said array.

Regarding claims 19 and 52, Choi et al. teach in figure 4B and related text a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated a space filled by a dielectric material. Prior art do not teach said space ranging from about 20 percent to about 50 percent of said surface area. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a space ranging from about 20 percent to about 50 percent of said surface area in prior art's device in order to reduce the size of the device (by providing a space ranging only from about 20 percent to about 50 percent of the total surface area) and by optimizing the characteristics of the device (by not proving the structures too close to each other which may degrade the device performance).

Regarding claims 35 and 53, prior art teach a capacitor electrically coupled with said first contact.

Claims 5-6, 34 and 46, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (6,566,704) and Ochipinti et al. (2004/0027889), as applied to claims 1, 35 and 43 above, and further in view of Farnworth et al. (6,515,325).

Regarding claims 5, 34 and 46, Choi et al. and Ochipinti et al. teach substantially the entire claimed structure, as applied to claims 1, 35 and 43 above, except explicitly stating that said first contact includes a catalyst pad characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube.

Farnworth et al. teach in figure 2A and related text (column 4, lines 32-50) a first contact includes a catalyst pad (by considering the first contact layer as layer 16, the catalyst pad is layer 16) characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first contact in prior art's device by including a catalyst pad characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube, in order to simplify the processing steps of making the device by using conventional growing method of semiconducting carbon nanotube.

Regarding claim 6, prior art's device includes said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance (the electrical-conductivity enhancing substance is the material of said at least one semiconducting carbon nanotube).

Regarding the process limitations recited in claims 5-6, 34 and 46 ("nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube", and "an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

Applicant argues that Choi et al. do not teach a gate dielectric disposed on the vertical sidewall of gate electrode, because gate dielectric 30 disposed above nanotube 100.

Figure 3F of Choi et al. clearly depicts gate dielectric 30 disposed on the vertical sidewall of gate electrode 20.

Applicant argues that "the channel region of each nanotube (100), which is between the source (40) and drain (50), is not disposed adjacent to a vertical sidewall of the gate electrode (20), as also required by Applicants' claim 1".

Figure 3F of Choi et al. clearly depicts the channel region of nanotube 100 disposed adjacent to a vertical sidewall of gate electrode 20, between the source 40 and drain 50 regions. It is unclear to the examiner why the channel region of nanotube 100 in Choi et al.'s structure is not disposed adjacent to a vertical sidewall of gate electrode 20.

Applicant argues that an artisan would not be motivated to modify figure 3F of Choi be the teachings of figure 4B of Choi, because the modification would require rearranging the gate dielectric, the gate electrode and the drain.

The examiner does not suggest to re-arrange the elements of the embodiment o figure 3F according to the embodiment of figure 4B of Choi. The embodiment of figure 4B is cited to merely teach an artisan that each of said semiconductor device structures

is arranged as an interconnected plurality of semiconductor device structures in an array characterized by a plurality of rows and a plurality of columns. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an array characterized by a plurality of rows and a plurality of columns in the embodiment of figure 3F of Choi et al.'s device in order to use the device in a practical application which requires plurality of unit cells and in order to simplify the processing steps of making the device by using conventional rows and columns array matrix.

Applicant argues that "Choi fails to disclose a device construction in which each of the semiconductor device structures includes a plurality of semiconducting carbon nanotubes, as set forth in claim 1".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the above features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to the examiner's statement, applicant argues that "there is no reasonable expectation of success that the device structure in Figure 3F could be modified as suggested by the Examiner. The Examiner's oversimplification fails to address the additional structural modifications that a person having ordinary skill in the art would have made to the device structure of Figure 3F of Choi in order to arrange a

plurality of the devices structures depicted in Figure 3F as a plurality of interconnected device structures and, that even if the rearrangement in the device construction were reasonably possible, each individual device structure still would not include multiple nanotubes. Even Choi sets forth the single nanotube device structure in Figure 3 and the interconnected device structures in separate and distinct embodiments in its written description, which a person having ordinary skill in the art would have interpreted to mean that the intrinsic evidence in Choi itself fails to demonstrate that there would have been a reasonable expectation of success to make the modifications suggested by the Examiner".

It is unclear to the examiner why "there is no reasonable expectation of success" to use the device structure in Figure 3F in an array structure. Forming a unit cell in an array arrangement is well known in the art. The formation is not "oversimplification" and does not require unknown "additional structural modifications" that a person having ordinary skill in the art is not familiar with.

Furthermore, regarding applicant's argument that "even if the rearrangement in the device construction were reasonably possible, each individual device structure still would not include multiple nanotubes", it is noted that each individual device structure does not need to include multiple nanotubes because this limitation is not recited in the rejected claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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